Clean Copy of Allowed Claims

1. A delay analysis system, executed on a computer, for making a delay analysis of a logic circuit, said delay analysis system comprising:

a delay analysis library comprising:

connection information and delay time information on rises and falls of input and output terminals for a plurality of circuits; and

for at least one circuit of said plurality of circuits, logical operation information between each input terminal and an output terminal of the logic circuit, the logical operation information being specified in a truth table in the library;

a delay analyzing module which computes delay times of the plurality of the circuits based on information in the delay analysis library,

wherein delay time for a signal path from input terminals to an output terminal of a logical circuit of said at least one circuit is computed based upon logical state transitions at said input terminals and a resulting logical state transition at said output terminal corresponding to the logical operation information,

wherein the delay time for a signal path from the input terminals to the output terminal of a logical circuit is computed by:

computing a sum of input terminal delay, delay between the input terminals and the output terminal and the output terminal delay for each combination of input and output terminals; and

selecting the delay time from the input terminals to the output terminal of the logical circuit from said sums of delays, wherein if a selected output terminal transitions from a low

state to a high state, said delay time is selected based on an input terminal whose logical transition triggers said low state to said high state transition at said selected output terminal according to the logical operation information, or if said selected output terminal transitions from a high state to a low state, said delay time is selected based on an input terminal whose logical transition triggers said high state to said low state transition at said selected output terminal according to the logical operation information,

wherein the delay analyzing module automatically computes the delay of the logical circuit based on the delay time information and the logical operation information in said delay analysis library.

2. A delay analysis system, executed on a computer, for making a delay analysis of a logic circuit, said system comprising:

a delay analysis library comprising:

connection information and delay time information on rises and falls of input and output terminals for a plurality of circuits; and

for each of said plurality of circuits, logical operation information between each input terminal and an output terminal of the logic circuit, the logical operation information being specified in a truth table in the library;

a delay analyzing module which computes delay times of the plurality of the circuits based on information in the delay analysis library,

wherein, respective delay time for a signal path from input terminals to an output terminal of a respective logical circuit of each of said plurality of circuits is computed based

upon logical state transitions at said input terminals and a resulting logical state transition at said output terminal corresponding to the respective logical operation information,

wherein the delay time for a signal path from the input terminals to the output terminal of the respective logical circuit is computed by:

computing a sum of input terminal delay, delay between the input terminals and the output terminal and the output terminal delay for each combination of input and output terminals; and

selecting the delay time from the input terminals to the output terminal of the respective logical circuit from said sums of delays, wherein if a selected output terminal transitions from a low state to a high state, said delay time is selected based on an input terminal whose logical transition triggers said low state to said high state transition at said selected output terminal according to the logical operation information, or if said selected output terminal transitions from a high state to a low state, said delay time is selected based on an input terminal whose logical transition triggers said high state to said low state transition at said selected output terminal according to the logical operation information,

wherein the delay analyzing module automatically computes the delay of the respective logical circuit of each of said plurality of circuits based on the respective delay time information and the logical operation information in said delay analysis library.

3. A computer-implemented method of making a delay analysis of a logical circuit, comprising:

referencing, using a computer, a delay analysis library for at least one circuit among a plurality of circuits, said delay analysis library comprising:

connection information, delay time information on rises and falls of input and output terminals for said plurality of circuits; and

for the at least one circuit among the plurality of circuits, logical operation information between each input terminal and an output terminal of the logic circuit, the logical operation information being specified in a truth table in the library;

computing by a delay analyzing module delay times for the at least one circuit of the plurality of the circuits based on information in the delay analysis library,

wherein, delay time for a signal path from input terminals to an output terminal for the at least one circuit among a plurality of circuits is computed based upon logical state transitions at said input terminals and a resulting logical state transition at said output terminal corresponding to the logical operation information,

wherein the delay time for a signal path from the input terminals to the output terminal for the at least one circuit among a plurality of circuits is computed by:

computing a sum of input terminal delay, delay between the input terminals and the output terminal and the output terminal delay for each combination of input and output terminals; and

automatically selecting a delay time from said sums of delays, wherein if a selected output terminal transitions from a low state to a high state, said delay time is selected based on an input terminal whose logical transition triggers said low state to said high state transition at said selected output terminal according to the logical operation information, or if said selected output terminal transitions from a high state to a low state, said delay time is selected based on an input terminal whose logical transition triggers said high state to said low state transition at said selected output terminal according to the logical operation information.

4. A computer-readable medium having stored thereon a program comprising computer instructions that, when executed on a computer, perform a process for executing a delay analysis method for a logic circuit, said computer-readable medium causing a computer to execute said method, wherein said method comprises:

referencing a delay analysis library for at least one circuit among a plurality of circuits, said delay analysis library comprising:

connection information, delay time information on rises and falls of input and output terminals for said plurality of circuits; and

for the at least one circuit among the plurality of circuits, logical operation information between each input terminal and an output terminal of the logic circuit, the logical operation information being specified in a truth table in the library;

computing by a delay analyzing module delay times for the at least one circuit of the plurality of the circuits based on information in the delay analysis library,

wherein, delay time for a signal path from input terminals to an output terminal for the at least one circuit among a plurality of circuits is computed based upon logical state transitions at said input terminals and a resulting logical state transition at said output terminal corresponding to the logical operation information,

wherein the delay time for a signal path from the input terminals to the output terminal for the at least one circuit among a plurality of circuits is computed by:

computing a sum of input terminal delay, delay between the input terminals and the output terminal and the output terminal delay for each combination of input and output terminals; and

automatically selecting a delay time from said sums of delays, wherein if a selected output terminal transitions from a low state to a high state, said delay time is selected based on an input terminal whose logical transition triggers said low state to said high state transition at said selected output terminal according to the logical operation information, or if said selected output terminal transitions from a high state to a low state, said delay time is selected based on an input terminal whose logical transition triggers said high state to said low state transition at said selected output terminal according to the logical operation information.

5. Canceled.

6. Canceled.